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⑭メモリ制御方式

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明 細 書

1. 発明の名称 メモリ制御方式

2. 特許請求の範囲

メモリのアクセスタイムが記入されるメモリアクセスタイム保持手段と、該メモリアクセスタイム保持手段にアクセスすべきメモリのアクセスタイムを記入するアクセスタイム記入手段と、上記メモリアクセスタイム保持手段に保持されたアクセスタイムの経過を検出する時間検出手段を具備し、上記アクセスタイム保持手段に保持されたメモリアクセスタイムが経過したときアクセスすべきメモリのメモリアクセスが終了したものと認識するようにしたことを特徴とするメモリ制御方式。

3. 発明の詳細な説明

本発明はメモリ制御方式に関し、特にアクセスタイムの異なる複数のメモリに対してもアクセス可能にしたメモリ制御方式に関するものである。

メモリ製造技術の大幅な進歩によりメモリ素子が大容量化され、ある程度のコスト低下が行なわれているものの、高速度メモリは依然として高価である。しかしながら一方では低速度のメモリは安くかつ大容量のものが得られるようになつている。また、データ処理速度を制御するとき、その融通性、拡張性、設計ミスの修正の容易性等の理由によりマイクロプログラムで制御するマイクロプログラミング制御方式がデータ処理装置の主流となつており、このためメモリがますます大容量化する傾向にある。

しかし、コストの観点という観点からみれば、メモリの記憶容量は大きくしたいが、すべてを高速化するのではなく、一部を高速素子で構成し、他を低速メモリ素子で構成し、例えば常駐プログラムのように使用頻度の高いものは高速メモリ素子に格納するという要求があり。したがつてこのような場合には動作速度の異なる複数のメモリ素子にアクセスすることが必要となる。

しかしながら従来使用されているメモリに対す

るインターフェイスとしては，①非同期インターフェイスとして，メモリ制御回路からメモリに対しリードスタート信号あるいはライトスタート信号を伝達し，メモリ側からメモリエンド信号が送出されたことによりメモリに対する書込み終了あるいは読出データ抽出終了を認識し，データを読出すという方式と，②同期インターフェイスとして，あらかじめ固定的に決められたプロセッサのサイクル数後にメモリの動作が終了するもの，例えばメモリからデータを読出す場合，あらかじめ例えば5サイクル後にデータがメモリから読出されるものと決定しておき，メモリに対してスタート信号発生後5サイクル後にデータを取りに行くというように動作を行なうという方式がある。

しかしこのような方式では，プロセッサのクロックに同期するための，非同期－同期化のため1クロックあるいは2クロック程度の同期化損失があり，また，クロック同期しない場合でも上記メモリエンド信号を受信するための回路が制御回路自体に必要となり，またメモリのアクセスタイムが変るとメモリ制御回路までが大幅に変更しなければならないという欠点がある。

したがつて本発明はこのような問題点を改善するとともに，アクセスタイムの異なるメモリにもアクセス可能とするメモリ制御方式を提供するものであり，このために本発明によるメモリ制御方式では，[illegible]メモリのアクセスタイムが記入されるメモリアクセスタイム保持手段と，該メモリアクセスタイム保持手段にアクセスすべきメモリのアクセスタイムを記入するアクセスタイム記入手段と，上記メモリアクセスタイム保持手段に保持されたアクセスタイムの経過を検出する時間検出手段を具備し，上記アクセスタイム保持手段に保持されたメモリアクセスタイムが経過したときアクセスすべきメモリのメモリアクセスが終了したものと認識するようにしたことを特徴とする。

以下本発明の一実施例を添付図面にもとづき説明する。

図は本発明の一実施例構成を示すものであつて，図中，1は第1制御メモリ，2は第2制御メモリ，3は制御メモリアドレスレジスタ，4はデコーダ，5はアンド回路，5'はオア回路，6は制御メモリ出力レジスタ，7はメモリアクセスサイクルカウンタ，8は減算カウンタ，9は「0」検出器，10は演算装置，11は固定値回路，12乃至18はアンド回路をそれぞれ示す。

第1制御メモリ1は，高速度でアクセスできるメモリであつて，使用頻度の高いマイクロプログラムが記入されている。第2制御メモリ2は，第1制御メモリ1よりは低速度のメモリであるが，しかし大容量のメモリであつて，第1制御メモリ1に記入されたもの以外のマイクロプログラムが記入されている。制御メモリアドレスレジスタ3は第1制御メモリ1または第2制御メモリ2のアドレス情報が記入される。このアドレス情報にはチップセレクト情報が含まれており，これをデコーダ4により解読し，その結果発信される選択信号CS0またはCS1により，上記第1制御メモリ1または第2制御メモリ2のいずれか一方が選択される。

メモリアクセスサイクルカウンタ7は，固定値回路11から伝達された一定値が記入されている。この一定値は，第1制御メモリ1のアクセスタイムに等しいクロック数が記入される。例えば第1制御メモリ1のアクセスタイムが100nsでありクロックの周期が30nsの場合には「5」が記入される。減算カウンタ8はクロックに応じてメモリアクセスサイクルカウンタ7に記入された数を－1するものであつて，例えば該メモリアクセスサイクルカウンタ7に「5」が記入されているとき，5クロック後には「0」が記入されることになる。そしてこの「0」が「0」検出器9により検出される。演算装置10は，第1制御メモリ1または第2制御メモリ2から読出したデータと外部回路条件等により演算を行ない，その結果得られた値をメモリアクセスサイクルカウンタ7にセットするものであり，この場合には固定値回路11から伝達された一定値とは別の値が記入される。

いま，初め第１制御メモリ１をアクセスする場合には，メイン・データ・バスから制御メモリアドレスレジスタ８にアドレス情報が記入される。そしてメモリアクセス制御信号（ＭＡＯＯ）Ⅰが「１」となりアンド回路１３がオン状態となり，固定値回路１１から供給された一定値がメモリアクセスインクリメンタ７に記入される。そしてメモリアクセススタート信号が「１」となりアンド回路16がオン状態となるので，メモリアクセスサイクルカウンタ７の値はクロックの印加毎に減算カウンタ８により－１される。この間に制御メモリアドレスレジスタ８に記入されたアドレス情報によりデコーダ６は選択信号ＯＳＯを「１」とし，第１制御メモリ１の指定されたアドレスに記入されたデータが読出される。そして上記減算カウンタ８により上記メモリアクセスサイクルカウンタ７が「０」になつたとき，これを「０」検出器９が検出して「１」を出力し，アンド回路５をオン状態にする。かくして第１制御メモリ１から読出されたデータがアンド回路５を経由して制御メモリ出力レジスタ６に出力される。そしてそのアドレス情報にもとづき次にアクセスすべき制御メモリのアドレス情報が制御メモリアドレスレジスタ８に記入され，また同時に各種制御信号が必要とするところに伝達される。これにより読出されたアドレス情報が再び第１制御メモリ１に対するものであれば，上記したような方式により，第１制御メモリ１が再びアクセスされる。

しかしながら次に読出したアドレス情報が第２制御メモリ２に対する場合には，まず，制御メモリアドレスレジスタ８に記入された該アドレス情報によりデコーダ６が選択信号ＯＳ１を「１」とし，第２制御メモリ２,Ｏ指定されたアドレスに記入されたデータが読出される。そしてメモリアクセス制御信号（ＭＡＯＯ）Ⅱが「１」となりアンド回路１４がオン状態となる。このとき，減算器１０が減算した，固定値回路１１から発生される一定値とは別の大きな数値が発生され，アンド回路１４を経由してメモリアクセスサイクルカウンタ７にセットされる。この値が，同様にして減算カウンタ８により「０」になつたとき「０」検出器９は「１」を出力する。そしてこのときに第２制御メモリ２から読出されたデータが制御メモリ出力レジスタ６に記入されることになる。このようなことが繰返され，第１制御メモリ１とはアクセスタイムの異なる第２制御メモリ２を必要に応じてアクセスすることができる。

勿論，そのときの条件に応じて，マイクロ命令による外部記入信号ＥＸＴＷを「１」にすれば，アンド回路１５がオン状態となり，マイクロ命令から与えられる定数ＯＳＤＲをローカルストア等よりメモリアクセスサイクルカウンタ７にセットすることもできる。また減算カウンタ８の代りに＋１カウンタを使用し，「０」検出器９の代りにメモリアクセスサイクルカウンタ７の値がある値になつたときに，アンド回路５をオンにするように構成することもできる。また，固定値回路１１に記入された数値を固定化せずに，例えば点線で示すサービスプロセッサ１６等より設定できるように構成し，第１制御メモリとしてそれまで使用していたものとは異なるアクセスタイムを有するものに取替えたような場合，この新しいものにあわせてその値を設定することも可能である。

以上説明した如く，本発明によれば，第１制御メモリと第２制御メモリのアクセスタイムが異なる場合でも，メモリインターフェイスは同期損失がなく，メモリアクセスサイクルカウンタにセットする値を変えるのみでよい。それ故，例えばマイクロプログラムを収容する制御メモリを，使用頻度の高いルーチンを高速の素子を使用した領域に記入し，それ以外のルーチンは低速の素子を使用した領域に記入する。そしてこの低速の素子を大容量のものとすれば，高速大容量の制御メモリを比較的低コストで得ることができる。また，制御メモリを全て低速素子で構成している場合に，一部のもののみを高速素子に使用することにより，高速の制御装置として使用することもできる。

更に，マイクロプログラム制御装置を各種用途に応じて，マイクロ命令の実行速度，マイクロプログラム量を適当に変えることも本発明を使用す

れば簡単になる。

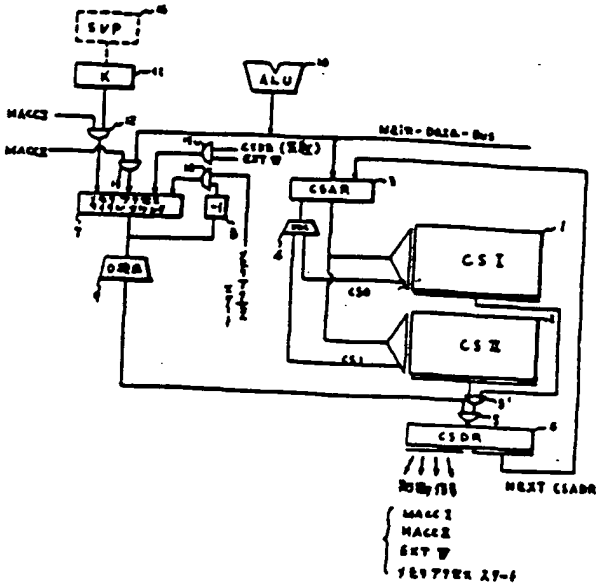
すなわち，コントロールメモリを大容量にしたい目的があり，コントロールメモリのアクセスタイムは多少遅くてもよい様な場合には，コントロールメモリ全体をアクセスタイムが速く，かつ大容量のものに変えても，制御装置の回路を変更することなく実現できる。

なお，以上の説明では制御メモリとして使用した例について説明したが，勿論本発明はこれのみに限定されるものではない。

4. 図面の簡単な説明

添付図面は本発明の一実施例構成を示す。

図中，1は第1制御メモリ，2は第2制御メモリ，3は制御メモリアドレスレジスタ，4はデコード，5はアンド回路，6は制御メモリ出力レジスタ，7はメモリアクセスサイクルカウンタ，8は減算カウンタ，9は「0」検出器，10は演算装置，11は固定値回路，12乃至15はアンド回路，16はサービスプロセッサをそれぞれ示す。



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(54) Memory control method

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Specification

1. Title of the Invention **Memory control method**

2. Claims

A memory control method characterized by being endowed with

a memory access time holding means in which the access time of the memory is entered, and

an access time entering means that enters the access time of the memory that should access said memory access time holding means, and

a time detection means that detects the passage of the access time held in the above-mentioned memory access time holding means, and

devised so that the memory access of the memory that should access when the memory access time held in the above-mentioned access time holding means has elapsed has ended is confirmed.

3. Detailed Description of the Invention

The present invention concerns a memory control method, particularly, a memory control method that has enabled access even with respect to a plurality of memory with different access times.

Due to great progress in memory manufacturing technology, memory devices have been made into mass storage devices, and although a lowering of costs, to some extent, is being carried out, high speed memory is as expensive as ever. However, on the other hand, the situation has developed so that inexpensive and, moreover, mass storage types of low speed memory can be obtained. And, when controlling data processing equipment, due to its versatility, expandability, easy of correcting design mistakes, and the like, a microprogramming control method that controls with a microprogram has become the main trend for data processing devices, and for this reason there is an increasing tendency for memory to be made mass storage.

However, if viewed from the viewpoint of cost reduction, an increase in memory storage capacity is wanted, but there is a demand not to make everything high-speed, but to constitute one part of high-speed memory devices and one part of low-speed memory devices, for example, to store in high-speed memory devices items that are used frequently such as resident programs. Consequently, in this type of case, accessing a plurality of memory devices of different operation speeds becomes necessary.

However, as interfaces with the memory used up to now there are: (1) as an asynchronous interface there is the method that transfers a read start signal or a write start signal to memory from a memory control circuit, and confirms the end of writing or the end of the extraction of read data, with respect to memory, by means of the fact that a memory end signal has been returned from the memory side, and reads out data, and (2) as a synchronous interface, the method that ends the operation of memory after the number of processor cycles permanently determined in advance, for example, when data is fetched from memory, it is decided, in advance, to read the data from memory after five

cycles, for example, and an operation is carried out to go and get data after five cycles after the generation of the start signal with respect to the memory.

However, with these kinds of methods there are the weak points that there is synchronization loss to the extent of the one clock or two clocks for asynchronization – synchronization, in order to synchronize the processor clock, and even when the clocks are not synchronized, a circuit for the purpose of receiving the above-mentioned memory end signal becomes necessary in the control circuit itself, and when the memory access times change, there must be great changes that extend to the memory control circuit.

Consequently, the present invention offers a memory control method to ameliorate these problems, and in addition, to enable access even to memory with different access times. For this purpose, the memory control method according to the present invention, is characterized by having [translator's note: several blacked out characters] a memory access time holding means with the memory access time entered, and an access time entering means that enters the access time of the memory that should be accessed, and a time detection means that detects the passage of the access time held in the above-mentioned memory access time holding means, and by being devised so as to confirm that when the memory access time held in the above-mentioned access time holding means has elapsed, the memory access of the memory that should be accessed has ended.

One embodiment of the present invention is explained below based on the attached drawing.

The drawing shows the constitution of one embodiment of the present invention. In the drawing, 1 indicates the number one control memory, 2 indicates the number two control memory, 3 indicates the control memory address register, 4 indicates the decoder, 5 indicates the AND circuit, 5' indicates the OR circuit, 6 indicates the control memory output register, 7 indicates the memory access cycle counter, 8 indicates the subtraction counter, 9 indicates the "0" detector, 10 indicates the arithmetic unit, 11 indicates the fixed value circuit and 12 to 15 indicate AND circuits.

The number one control memory 1 is a memory that can access at a high speed, and microprograms with a high frequency of use are entered. The second control memory 2 is a memory of a lower speed than the number one memory, but is a mass storage memory, and the microprograms other than those entered in the number one memory 1 are entered. The address information of the number one control memory 1 and the number two control memory 2 is entered in the control memory address register 3. Chip selection information is included in this address information, and this is explained by the decoder 4 and, by means of the selection signals CS0 or CS1 sent as a result, either the number one control memory 1 or the number two control memory 2 mentioned above is selected.

The memory access cycle counter 7 has a fixed value transferred from the fixed value circuit 11 entered. This fixed value has the number of clocks equivalent to the access time of the number one control memory 1 entered. For example, when the access time of the number one control memory 1 is 100 ns and the cycle of a clock is 20 ns, "5" is entered. The subtraction counter 8 reduces by -1 the number entered in the memory access cycle counter 7 in proportion to the clocks, for example, when said memory access cycle counter 7 has "5" entered, after five clocks "0" is entered. And, this "0" is detected by the

"0" detector 9. The arithmetic unit 10 carries out operations based on the data read out from the number one control memory 1 or the number two control memory 2 and the external circuit conditions, and the like, and the value obtained as a result is set in the memory access cycle counter 7, and in this case a value different from the fixed value transferred from the fixed value circuit 11 is entered.

Now, first, when the number one control memory 1 is accessed, address information is entered in the control memory address register 3 from the main database. And then the memory access control signal (MACC) I becomes "1" and the AND circuit 12 attains the ON state, and the fixed value transferred from the fixed value circuit 11 is entered in the memory access cycle counter 7. And since the memory access start signal becomes "1" and the AND circuit 14 attains the ON state, the value of the memory access cycle counter 7 is made –1 [Tr.note: reduced by 1?] by the subtraction counter 8, for every impression of the clock. During this time the decoder 4 set the selection signal CS0 to "1" according to the address information entered in the control memory address register 3, and the data entered in the address designated by the number one control memory 1 is read. And then, when the above-mentioned memory access cycle counter 7 has become "0" due to the above-mentioned subtraction counter 8, the "0" detector 9 detects this, outputs "1" and places the AND circuit 5 in the ON state. In this way the data read from the number one control memory 1 is output to the control memory output register 6 by way of the AND circuit 5. And, based on that address information, the address information of the control memory that should be accessed next is entered in the control memory address register 3, and at the same time various control signals are transmitted to the necessary places. If the address information read by means of this is in the number one control memory 1 again, by means of the method mentioned above, the number one control memory 1 is accessed again.

However, when the address information that is read next is in the number two control memory 2, first, the decoder 4 sets the selection signal CS1 to "1" by means of said address information entered in the control memory address register 3, and the data entered in the address designated by the number two control memory 2 is read. And, the memory access control signal (MACC) II becomes "1" and the AND circuit 18 attains the ON state. At this time, a large numerical value that is different from the fixed value which the arithmetic unit 10 computed and which was generated from the fixed value circuit 11, was generated and set in the memory access cycle counter 7 by way of the AND circuit 18.

When this value has become "0" due to the subtraction counter 8, in the same way, the "0" detector 9 outputs "1". And, the data read from the number two control memory 2 at this time becomes entered in the control memory output register 6. This type of activity can be repeated and a number two control memory 2 with an access time that differs from that of the number one control memory 1 can be accessed when necessary.

Of course, if, in response to the conditions at that time, due to a microcommand an external entered signal EXTW is made "1", the AND circuit 15 attains the ON status, and the constant CSDR given from the microcommand can also be set in the memory access cycle counter 7 from the local store, and the like. And, when the +1 counter is used instead of the subtraction counter 8, and the value of the memory access cycle counter 7,

instead of the "0" detector 9, has become a certain value, the AND circuit 5 can also be configured so as to attain the ON state. And, when changed to one that has an access time that is different from that used up to then as the number one control memory, without fixing the numerical value entered in the fixed value circuit 11, for example, configuring so that it can be set from the service processor 16, and the like, shown by the dotted line, that value can also be set in line with this new one.

As explained above, according to the present invention, even if the access times of the number one control memory and the number two control memory differ, the memory interface does not have a synchronization loss, and is acceptable by simply changing the value set in the memory access cycle counter. For that reason, the control memory that accommodates a microprogram, for example, enters routines with a high frequency of use in a region that uses a high-speed device, and the other routines are entered in a region that uses a low-speed device. And if this low-speed device is made one of mass storage, ultimately, control memory of mass storage can be obtained at a comparatively low cost. And, when all the control memory is constituted of a low-speed device, it can also be used as a high-speed control device by using only one part in a high-speed device.

Furthermore, appropriately changing the execution speed of microcommands and the microprogram quantity of the microprogram control device in response to various uses also becomes simple, if the present invention is used.

That is, there is the objective to want to make the control memory mass storage, and in the kind of case in which the access time of the control memory is acceptable, even when it is somewhat slow, it can be realized without changing the circuit of the control device, even if the access time of the entire control memory is slow and is changed to one of mass storage.

Furthermore, in the above explanation an example used as control memory was explained, but, of course, the present invention is not limited to this only.

4. Brief Description of the Drawings

The attached drawing shows the constitution of one embodiment of the present invention.

In the drawing: 1 indicates the number one control memory; 2 indicates the number 2 control memory; 3 indicates the memory address register; 4 indicates the decoder; 5 indicates the AND circuit; 6 indicates the memory output register; 7 indicates the memory access cycle counter; 8 indicates the subtraction counter; 9 indicates the "0" detector; 10 indicates the arithmetic unit; 11 indicates the fixed value circuit; 12 to 15 indicate AND circuits; 16 indicates the service processor.

[in the drawing]

[line coming from 15] (CSDR) (constant)

[line coming from 14] memory access start

[lower right, from CSDR] control signals

MACCI, MACCII, EXTW, memory access start

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(54) Memory storage device

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(22) Patent Application Filing Date: July 2, 1980

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Specification

1. Title of the Invention

Memory storage device

2. Claims

In a memory storage device that operates synchronized to the master clock of a central processing unit, a memory storage device characterized by the fact that multiple groups of

a clock selector that selects from the above-mentioned master clock an interface signal receiving and sending clock, and due to the fact that the selection conditions of said clocks are established from the outside,

a configuration control register that controls the above-mentioned clock selector by said selection conditions are provided.

3. Detailed Description of the Invention

The present invention relates to a memory storage device (hereafter referred to as "MS"), particularly, one related to an MS that can freely select the receiving and sending clocks of the interface signal.

In an MS that carries out the receiving and sending operations of the interface signal synchronized with the master clock of the central processing unit (hereafter referred to as "CPU"), taking into consideration the delay due to the machine cycles of the CPU, as well as the length of the cable between the CPU and the MS, and the like, the transfer time between the CPU and the MS is decided among any of 1/4, 2/4, 3/4 or 4/4 machine cycles, and the like.

After that, the MS decides the interface signal receiving and sending clock based on the sending and receiving time of the interface signal in the CPU, and furthermore, the transfer time decided as mentioned above.

FIG. 1 is a connection diagram of the conventional MS and CPU.

In MS1 an interface receiving latch 2, an interface sending latch 3, a control part 4 and a memory part 5 are provided and connected to the CPU 6 via the interface receiving latch 2 and sending latch 3.

The n interface signals S_i (1 – n) transferred from the CPU 6 are latched to the interface receiving latch 2 by the respective clock signals ti. The control part 4 and the memory part 5 operate according to this latch information.

The interface sending latch 3 sends the report information of this series of operations to the CPU 6 as m interface signals S_o (1 – m) according to the clock signal tj.

In the case of FIG. 1, as for the latch clocks ti, tj of the interface receiving latch 2 and the interface sending latch 3, the respective clocks divided from the clock generating part 10 of the CPU 6 are used, and with respect to the sending and receiving clocks of the

interface signal in the CPU 6, clocks that have shifted only the transfer time (1/4, 2/4, 3/4 or 4/4 machine cycles, and the like) between the CPU 6 and the MS1 are used.

In this way, because up to now the interface signal receiving and sending clocks in the MS are fixed by the hardware, when a change of the machine cycle and a change of the connection group length has occurred, a large scale change of the hardware is necessary. Furthermore, sharing the MS is impossible by other CPUs which have different machine cycles or connection cable lengths, and a MS becomes exclusively used for a specific CPU.

The purpose of the present invention is to offer an MS that gives a logical degree of freedom to the time relationship of the interface system and makes possible a connection to many types of CPUs that have different machine cycles as well as a change of the time relationship of the interface system, without changing the hardware, in order to solve the above-mentioned conventional problem.

The MS of the present invention is characterized by the fact that it provides multiple selectors for selecting clocks that decide the timing of the receiving and sending of the interface signal, and forming a pair with these selectors, configuration control registers that control the selection condition of the selectors, and select the interface signal receiving and sending clocks by writing control information from the outside to these configuration control registers.

Below, the embodiment of the present invention is explained by means of FIG. 2.

MS1, the same as formerly, provides an interface receiving latch 2, an interface sending latch 3, a control part 4 and a memory part 5 connected to a CPU 6. The n interface signals S_i (1 – n) sent from the CPU 6 are latched to the interface receiving latch 2 by each clock signal *ti*. The control part 4 and the memory part 5 operate according to this latch information.

The interface receiving latch 3 sends the report information of this series of operations to the CPU 6 as *m* interface signals S_o(1 – m) by means of a clock signal *tj*.

MS1, besides these, is provided with a configuration control register 7 and a clock selector 8, and the latch clocks of the interface receiving latch 2 and the interface sending latch 3 each receive the clocks *ti* or *tj* logically selected by the clock selector 8. Furthermore, the logical clock selection based on this clock selector 8 is controlled by the configuration control register 7. Furthermore, the writing in of the selection conditions to the configuration control register 7 can be executed by various methods such as scanning in or the operation of a switch of a panel.

Furthermore, with respect to the input/output interface signals, multiple sets of the configuration control register 7 and the clock selector 8 of these have been prepared, and by the writing in to each configuration control register 7, logically and freely selecting the receiving and sending clocks of the interface signal is possible.

As explained above, according to the present invention, because the receiving and sending clocks of the interface signals of the MS can be logically and freely selected, the sharing of the MS by CPUs that have different machine cycles or connection cable

lengths is possible, and in the state of being connected to a specific CPU, there is no necessity to change the hardware at the time of a change of the machine cycles, a change of the connection cable length, or a change of the performance of the memory device. Moreover, the clock signal can be changed experimentally, and a marginal test of the interface signal can be carried out simply.

4. Brief Description of the Drawings

FIG. 1 is a connection diagram of the conventional MS and CPU; FIG. 2 is a connection diagram of the MS and CPU that shows the embodiment of the present invention.

1 memory storage device (MS)

2 interface receiving latch

3 interface sending latch

4 control part

5 memory part

6 central processing unit (CPU)

7 configuration control register

8 clock selector

10 clock generating part

to – 3 master clock

$S_i(1 - n)$ interface receiving signal

$S_i(1 - m)$ interface sending signal

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FIG. 1

FIG. 2